REMARKS

Entry of this Amendment is proposed because it does not raise any new issues requiring further search, narrows the issues on appeal and does not require further search by the Examiner.

Claims 5, 7, 8, and 21 are presently pending in the application.

Applicants note that the Office Action indicates that claim 21 should be canceled (see Office Action at page 2, numbered paragraph 1). Also, the Office Action indicates that the final rejection is based on claims 5, 7, 8, and 19. However, these appear to be typographical errors, since claims 5, 7, 8, and 21 (i.e., Group I in the Restriction Requirement dated February 26, 2003) were elected for prosecution on the merits in the Response to Restriction Requirement filed on March 24, 2003. Also, claims 5, 7, 8, and 21 properly have been considered in the present Office Action.

Accordingly, claims 18 and 19 have been canceled without prejudice or disclaimer, and as mentioned above, claims 5, 7, 8, and 21 are pending.

It is noted that the claim amendments are made only for canceling non-elected claims, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 5, 7, 8, and 21 stand rejected under 35 U.S.C. §112, first paragraph, and under 35 U.S.C. §112, second paragraph.

These rejections are respectfully traversed in the following discussion.

I. THE 35 U.S.C. § 112, FIRST PARAGRAPH REJECTION

Claims 5, 7, 8, and 21 stand rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement. Applicants respectfully traverse this rejection, for the following reasons.

Applicants submit that the ordinarily skilled artisan could certainly practice (e.g., make and use) the claimed invention of a "method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state" after a thorough reading of the specification with reference to the drawings, and therefore, respectfully traverses this rejection.

For the Examiner's convenience, Applicants remarks submitted in the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004 are incorporated herein by reference.

The Examiner has alleged in the non-final Office Action dated November 10, 2003, that the Specification does not disclose a clear meaning of the term "test sweep." The Examiner also has stated that it is confusing what a "test sweep" does, since the definition of a "test sweep" and the scope its application allegedly is unknown. Moreover, the Examiner has alleged that a "test sweep" is not a common term in the art (see Office Action at pages 2-3, numbered paragraph 3).

In the present Office Action, the Examiner acknowledges that "*Applicant has defined what a test sweep is*" (as set forth in the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004) but alleges that such "*is insufficient to clarify the meaning in the claims*" (see Office Action at page 3, numbered paragraph 7, Remarks; emphasis added).

Applicants respectfully disagree.

As specifically acknowledged by the Examiner, Applicants have identified for the Examiner the specific examples in the original specification that explain and define this feature

of the claimed invention (see Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004 at pages 6-8).

That is, as mentioned above, the Examiner specifically acknowledged that "*Applicant has defined what a test sweep is*" (see Office Action at page 3, numbered paragraph 7, Remarks; emphasis added).

Thus, it is unclear *how* the clear explanation and definition of this feature, as defined in the original disclosure, could be "*insufficient to clarify the meaning in the claims*" (see Office Action at page 3, numbered paragraph 7, Remarks; emphasis added).

Again, Applicants respectfully disagree.

As mentioned above, Applicants have complied with all of the requirements for establishing the enablement of the claimed invention, and moreover, have specifically identified for the Examiner the corresponding description in the original specification of the disputed claimed feature, and have provided a clear explanation and clarification for the Examiner, thereby clearly rebutting the Examiner's position.

The Examiner respectfully is requested to reconsider the specific rebuttal arguments at pages 6-8 of the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004, in response to the Examiner's comments.

Applicants note that, as ample case law has held, the test for enablement is whether one of ordinary skill in the art could practice (e.g., make and use) the invention (e.g., the claimed invention), without undue experimentation.

Applicants respectfully submit that a *prima facie* case has not been established by the Examiner.

That is, the Examiner has not established the specific reasons *why* one of ordinary skill in the art could not practice (i.e., make and use) the claimed invention, which is directed to a "method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state", without undue experimentation.

As mentioned above, in the Office Action, the Examiner merely states that "*Applicant has defined what a test sweep is*" but that "it is *insufficient to clarify the meaning in the claims*" (see Office Action at page 3, numbered paragraph 7, Remarks; emphasis added).

However, as Applicants identified in the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004, the specification specifically describes that:

> [T]he Auto_Don't_Care method searches the database (e.g., table, etc.), to locate all tests that have this function (e.g., the function of the control signal) and creates a test sweep (e.g., as shown in step 46 described below)

(see specification at page 17, lines 19-21; see also Figures 4A and 4B).

Indeed, the original specification explains, in detail, the operation of an exemplary embodiment of the claimed method, with reference to Figures 4A and 4B (e.g., see specification at page 17, line 17, to page 20, line 2).

It is incumbent on the Examiner to explain *why* it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement (e.g., see M.P.E.P. § 2164.04; see also In re Marzocchi, 169 USPQ 367, 370 (CCPA 1971)).

Moreover, the Examiner should identify *what* information is missing and *why* one skilled in the art could not supply the missing information without undue experimentation (e.g., see M.P.E.P. § 2164.04 and § 2164.06(a)).

Applicants respectfully submit that the Examiner's conclusory statements do not meet the basic requirements for establishing a *prima facie* case of lack of enablement.

On the other hand, even assuming *arguendo* that a *prima facie* case was made that one of ordinary skill in the art, taking the present invention as a whole, would not have been able to make and use "a method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state" without undue experimentation, to overcome a *prima facie* case of lack of enablement, Applicant must demonstrate by argument and/or evidence that the disclosure, as filed, would have enabled the claimed invention for one skilled in the art at the time of filing (see M.P.E.P. § 2164.05).

Applicants have specifically identified and explained for the Examiner the corresponding description in the original specification of the disputed claimed structure, thereby clearly rebutting the Examiner's position (see Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004 at pages 6-8).

In light of the specific examples in the original disclosure, Applicants submit that the ordinarily skilled artisan could certainly make and use the claimed invention of "a method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state" after a thorough reading of the specification with reference to the drawings.

In other words, one of ordinary skill in the art could practice (e.g., make and use) the invention, without undue experimentation.

Accordingly, Applicants respectfully request that the Examiner withdraw this rejection and permit these claims to pass to immediate allowance.

II. THE 35 U.S.C. § 112, SECOND PARAGRAPH REJECTION

Claims 5, 7, 8, and 21 stand rejected under 35 U.S.C. §112, second paragraph, as being incomplete for allegedly omitting essential cooperative relationships of elements, and that such alleged omissions amount to a gap between the necessary structural connections.

With respect to independent claims 5 and 21, the Examiner alleges that, if Applicants' explanation of "test sweep", as set forth in the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004, were to be relied upon, then the claims allegedly would lack a structural/functional relationship between the "test sweep", template, and the remaining claim limitations (see Office Action at page 3, numbered paragraph 5).

Applicants respectfully disagree with the Examiner's position and submit that a person of ordinary skill in the art clearly would know the metes and bounds of the subject matter of claims 5, 7, 8, and 21.

As emphasized below, independent claims 5 and 21 clearly and particularly define each of the claimed elements with reference to at least the control signals.

For example, independent claim 5 recites a method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state, comprising:

> automatically reading and setting a state value of control signals on a per-cycle basis in a template and updating the HDL design with new data;
> changing a first predetermined value of the template to be set with the previous cycle state of the control signals; and
> executing a test sweep to determine a "don't care" state of the control signals (emphasis added).

On the other hand, independent claim 21 somewhat similarly recites a signal-bearing medium tangibly embodying a program of machine readable instructions executed by an apparatus to perform a method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state, said method comprising:

> automatically reading and setting a value of control signals on a per-cycle basis in a template and updating the HDL design with new data;
> changing a first predetermined value of the template to be set with the previous cycle state of a control signal; and
> executing a test sweep to determine a "don't care" state of the control signals (emphasis added).

Thus, the claims clearly do not lack structural/functional relationships between the test sweep, template, and the remaining claim limitations, as alleged by the Examiner (see Office Action at page 3, numbered paragraph 5).

Moreover, Applicants clearly and particularly describe the features of an illustrative embodiment of the claimed invention in the original specification, as explained to the Examiner in the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004, at pages 8-10).

For example, the Specification clearly describes an exemplary embodiment of the claimed invention, i.e., an "Auto_Don't_Care" method of design, as,

> [t]he Auto_Don't_Care method searches the database (e.g., table, etc.), to locate all tests that have this function (e.g., the function of the control signal) and creates a test sweep (e.g., as shown in step 46 described below)
>
> In this way, the process modifies the design so as to always set in the current cycle all control signals input to their active values. The purpose of such a step is ultimately to set the control bits of an opcode which does not change (e.g., has no affect) to a "don't care" value.
>
> Hence, the new template (e.g., the modified design) updates the temporary copy of the updated microcode function block, and then, as shown in step 46, a test sweep is run with the previous state set for the one control signal being examined currently.

(see specification at page 17, lines 19-29; emphasis added).

As Applicants described in the Amendment under 37 C.F.R. § 1.111 filed on February 10, 2004, all of the templates are then executed on the microcodes together with each other. Again the HLLE ensures that the previous control signals are always in the true state (e.g., overrides values). In step S51, a full regression analysis is executed to ensure that the opcode function still functions with the automatically-generated "don't care" verilog (e.g., with the "don't care" bits set). As mentioned above, the regression is a list (or set) of architectural test cases which are supplied to verify the microprocessor design (e.g., see specification at page 18, line 26 to page 19, line 3).

In other words, as would be well known to one of ordinary skill in the art, the ADC method identifies or marks those control lines which need not be toggled between a previous cycle and a current cycle as a potential "don't care".

Thus, when the ADC method runs all of its test sweeps, the identity of those "don't care" lines is used to update the hardware description language, so that the amount of logic circuitry associated the ADC method can be minimized.

Hence, as would be obvious to one of ordinary skill in the art, the relationship between the control signals and the new data of independent claim 5 (and somewhat similarly, independent claim 21), is that of identifying particular control signals as a potential "don't care" state and using this new data to update the hardware description language with an end result of minimizing the architectural logic circuitry for the microprocessor design.

Thus, Applicants respectfully submit that a person of ordinary skill in the art clearly would know the metes and bounds of the subject matter of claims 5, 7, 8, and 21, and that these claims do not lack a structural/functional relationships between the claimed features, as alleged by the Examiner.

Indeed, the Examiner has not explained *how* or *why* such features of the claimed invention lack structural/functional relationships between one another, but instead, merely states that such is the case.

As the Examiner well knows, whenever possible, the Examiner should make the record clear by providing explicit reasoning for making or withdrawing any rejection related to 35 U.S.C. § 112, second paragraph (e.g., see M.P.E.P. § 2173.02, last paragraph).

Applicants respectfully submit, however, that mere conclusory statements without more (as in the present Office Action) are not sufficient to establish a reasonable ground of rejection under 35 U.S.C. § 112, second paragraph.

Therefore, for at least the foregoing reasons, Applicants respectfully submit that claims 5, 7, 8, and 21 do not omit essential structural cooperative relationships of the invention and

instead, particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Accordingly, Applicants respectfully request that the Examiner withdraw this rejection and permit these claims to pass to immediate allowance.

III. FORMAL MATTERS AND CONCLUSION

In the Examiner's Remarks (see Office Action at page 3, numbered paragraph 8), the Examiner alleges that the proposed specification (title) amendment does not comply with Patent Office procedures, and therefore, no Title change has been entered.

Therefore, Applicants have amended the Title of the Invention herewith, in accordance with Patent Office procedures and accordingly, respectfully request entry of the same and withdrawal of the objection.

Applicants also note that an Information Disclosure Statement was filed on May 20, 2004 (subsequent to the present Office Action), and respectfully request that the Examiner kindly consider the references cited therein and provide a signed and initialed form PTO 1449.

In view of the foregoing, Applicant submits that claims 5, 7, 8, and 21, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: July 6, 2004

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CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 the enclosed Amendment under 37 C.F.R. § 1.116 to Examiner Annette M. Thompson on July 6, 2004.

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RE-SUBMISSION:
NO EXTENSION
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